



SHAPING THE NEXT GENERATION OF ELECTRONICS

JUNE 23-27, 2024

MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA





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Timing Robustness: A Way forward for analyzing timing-voltage sensitive paths for accounting IR-Drop Variations

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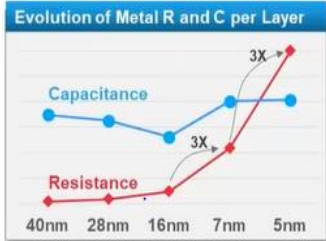
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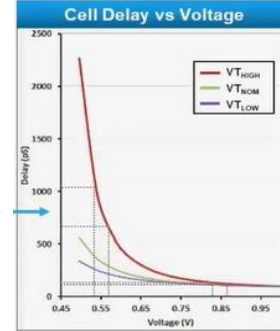


Motivation

- IR drop is the voltage drop in the metal wires constituting the power grid
- As technology node shrinks, Resistance dominates the impact on cell-delays



- R has increased from 28nm to 7nm by 10x
- RC constant is dominated by R

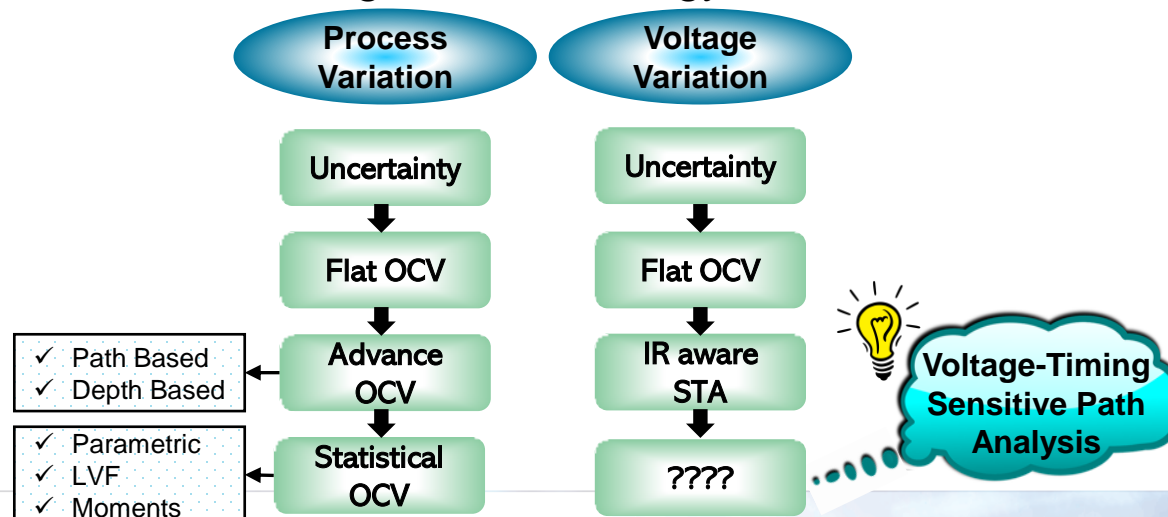


- dt/dV is much steeper at low voltages
- Cell delays are non-linear with IR drop

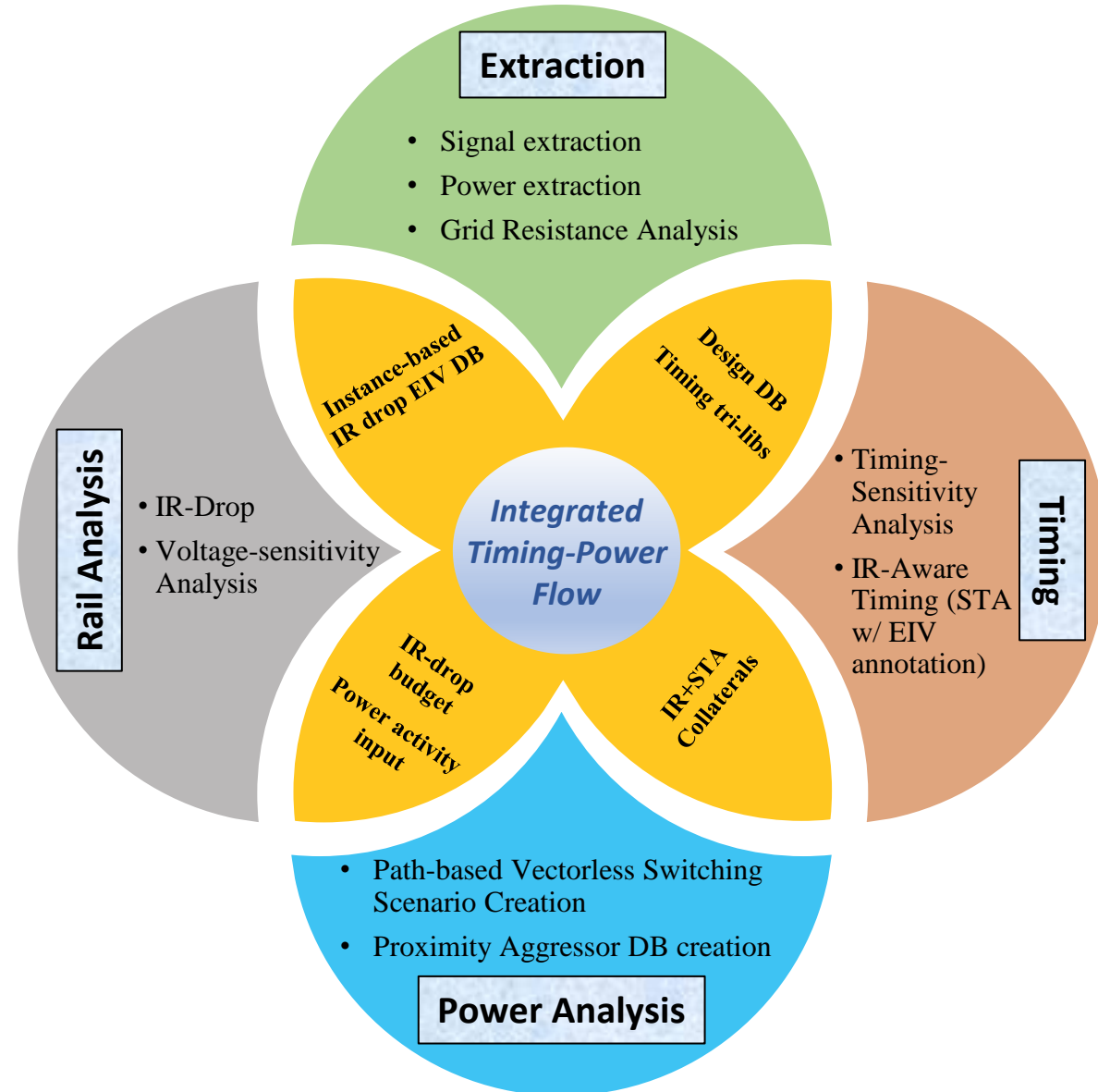
- Devices designed on lower technology node are focused primarily for
 - Small pessimism added due to over-constrained local variation handling can cause higher design closure time, or increased power/area due to over-fixing
- Evolution of Local Variation handling with technology node:

High Operating Frequency

Low Power/Area



Main Idea



Timing-Voltage Sensitivity analysis

- Ranking timing paths in the design based on paths' voltage sensitivity and timing criticality
- Higher the delay variation with respect to voltage (dt/dv), higher is the voltage-sensitivity
- Ranking = $\text{func}(dt/dv, \text{setup-slack})$

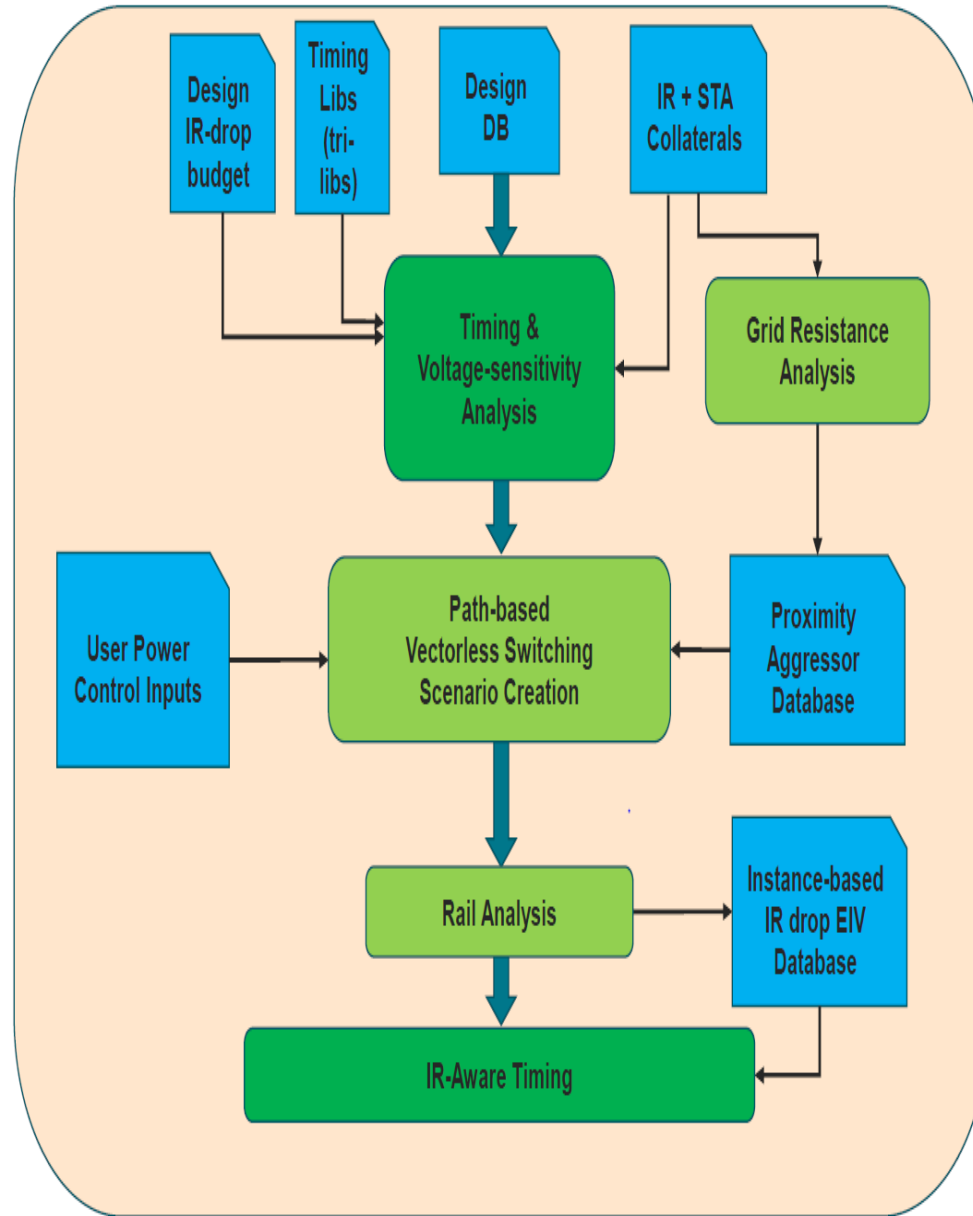
Path-based vectorless switching scenario creation

- Dividing the design into multiple physical grids
- Scheduling endpoints (based on sensitivity ranking) in each grid in every alternate cycle
- Maintaining same sequential activity across cycles, along with grid-based scheduling ensures temporal and spatial uniformity

Proximity Aggressor creation

- Identifying & toggling, IR aggressor(s) to critical instances along-with, honoring TW overlap

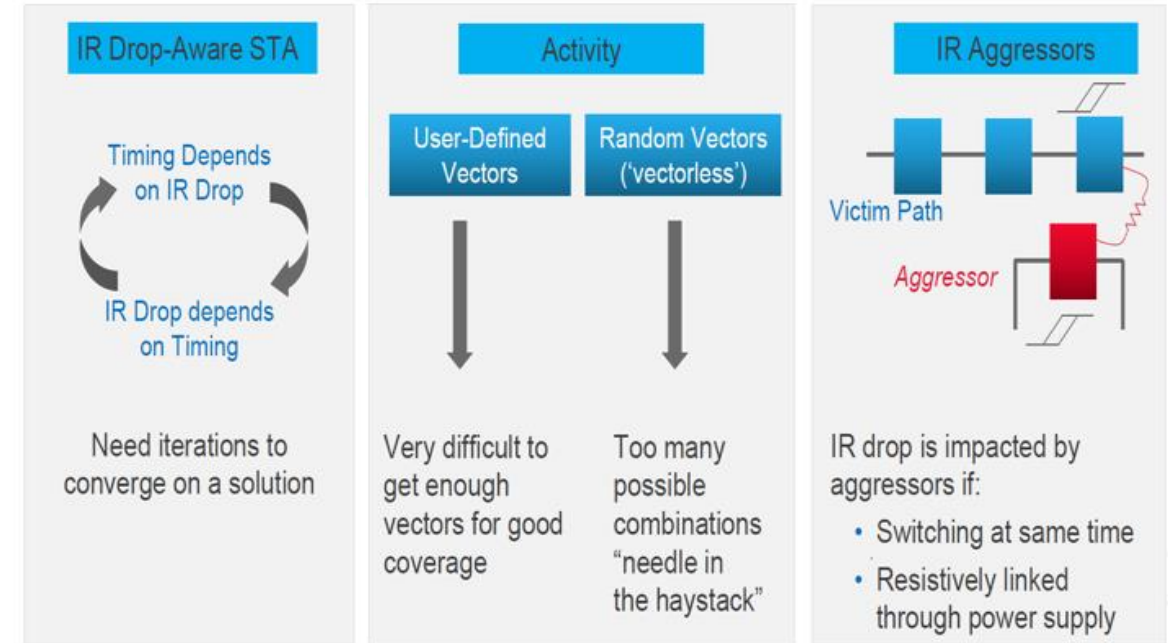
Integrated Timing-Power Flow Methodology



Advantages

Traditional IR aware STA Flow

- **Separate Timing and Voltage analysis:**
 - Run IR analysis on Power-Integrity (PI) tool and generate Effective Instance Voltage (EIV) file
 - Back-annotate EIV files in STA tool and run timing
 - Requires iterations to converge on a solution, and impacts design cycle-time
 - **Proposed Flow, performs timing and voltage analysis under a common cockpit**
- **Activity Selection:**
 - Vectored analysis: Difficult to get a best-case vector for dynamic solution
 - Vectorless analysis: Focuses on design coverage
 - **Proposed Flow, uses a more directed vectorless approach, with priority to timing-voltage sensitive paths, followed by full design coverage**
- **IR Aggressors:**
 - **Proposed Flow, uses Timing-Window overlap for identifying IR aggressors, linked to victim through resistive power supply**



Results

Design Info

Instance count	~90M
Technology node	TSMC 5nm (N5)
Timing corner	SSGNP/0.675v/0c/rcworstCCwT0c
Tri-libs	SSGNP/0.585v-0.675v-0.765v/0c
Power corner	TT/0.75v/85c/typical85c
Estimated IR-Drop factor	Package: 5% Drop: 10%
Switching activity <ul style="list-style-type: none">- input activity- sequential activity- clock-gate activity- macro activity- time period	60% 60% 200% 10% 416ps (2.4GHz)
Node count (vdd+vss)	1.36B

Flat Voltage Derate Run

- STA @ SS/0.675v/0c
- Operating Voltage 0.675v
- 0.675v .libs
- Voltage Derates
- Temperature Derates

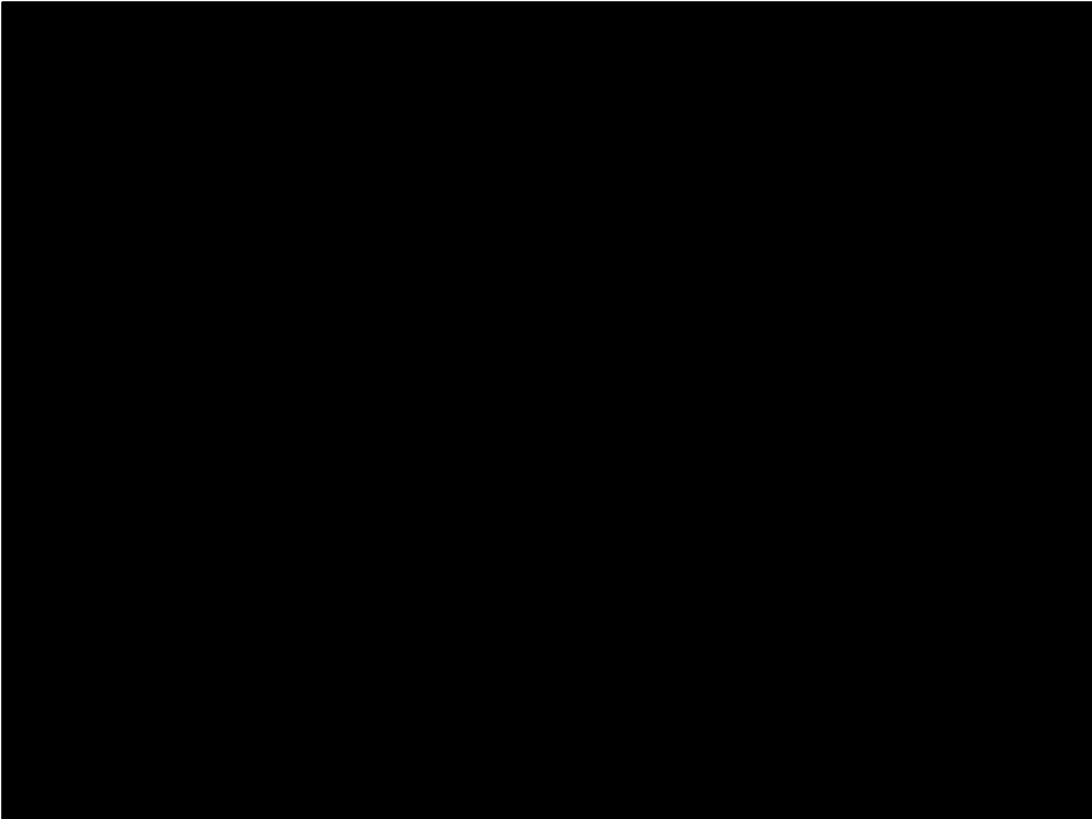
Integrated Timing-Power Run

- STA @ SS/0.75v/0c
- Operating Voltage 0.75v
- Tri-lib setup 0.585v-0.675v-0.765v .libs
- IR budget
- Effective Instance Voltage drop (EIV) files annotated during STA
- Temperature Derates

No Voltage Variation Run

- STA @ SS/0.75v/0c
- Operating Voltage 0.75v
- Tri-lib setup 0.585v-0.675v-0.765v .libs
- Temperature Derates

Results (contd.)



99.9% of instances are within
IR margin of 75mV

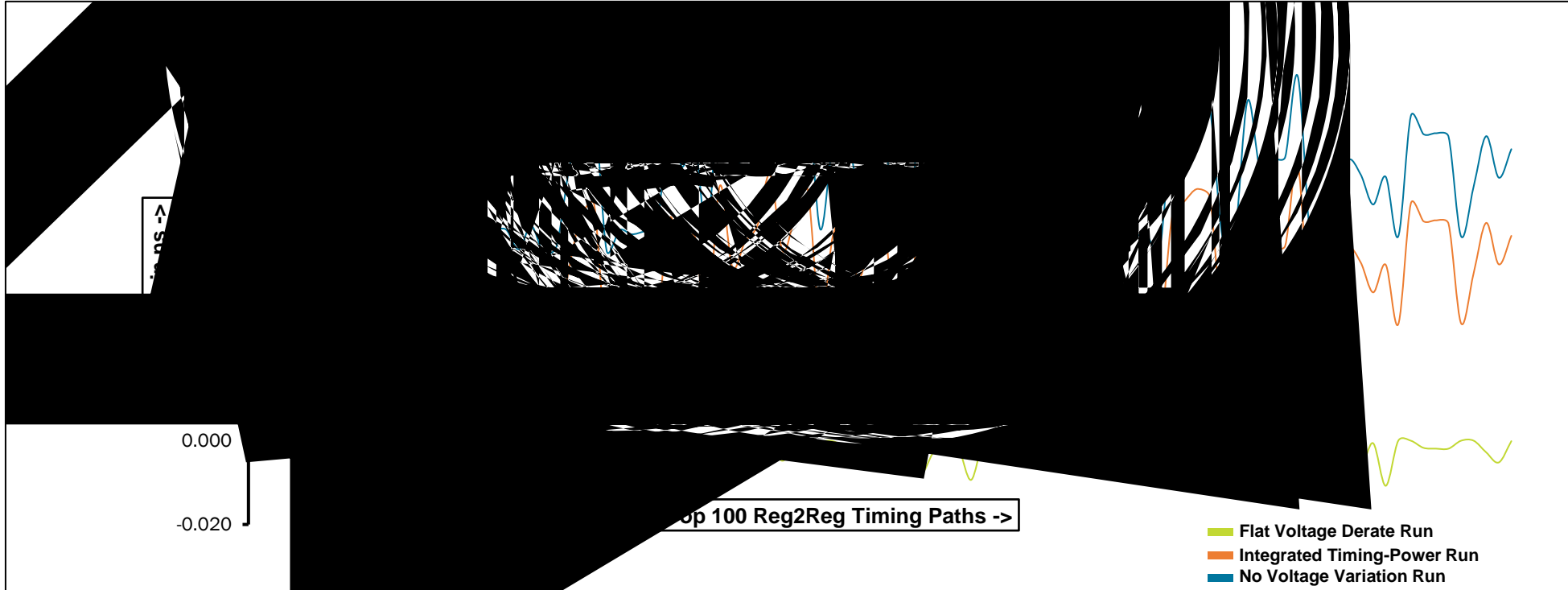
Flat Voltage Derate Run	All	In2Reg	Reg2Reg	Reg2Out
WNS (ns)	-1.005	0.0	-0.016	-1.005
TNS (ns)	-15721.7	0.0	-3.3	-15718.4
VP	19839	0	1781	18058

Integrated Timing-Power Run	All	In2Reg	Reg2Reg	Reg2Out
WNS (ns)	-0.949	0.0	0.0	-0.949
TNS (ns)	-14847.1	0.0	0.0	-14847.1
VP	18058	0	0	18058

No Voltage Variation Run	All	In2Reg	Reg2Reg	Reg2Out
WNS (ns)	-0.879	0.0	0.0	-0.879
TNS (ns)	-13740.5	0.0	0.0	-13740.5
VP	18058	0	0	18058

Setup Timing Summary across runs

Evidence



- Flat voltage derate run is at Slow corner Nominal -10% voltage, with added flat voltage derates for accounting IR-Drop
- No voltage variation run is at Slow corner Nominal voltage using TRI-Libs (0.585v/0.675v/0.765v) with no flat IR-Drop derates
- Proposed Integrated Timing-Power flow run is at Slow corner Nominal voltage with EIV annotations and no IR-Drop derates
- From the graph it is clear, that Reference run shows higher pessimism and over constrains the design
- Integrated Timing-Power run shows realistic timing numbers when compared to Reference run where flat voltage derates were applied

Conclusion and Future work

- Proposed Timing-Power Integrated Flow, was able to model IR induced slack degradations
- STA signoff margins are conservative enough to cover these degradations
- Proposed Timing-Power Integrated Flow, can be used to waive timing violations in STA due to tighter flat voltage derates
- Timing violation waiver can further help in reducing ECO iterations for design closure
- Performing Full Chip level STA analysis with proposed flow
- Performing Timing ECOs with EIV annotations

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THANK YOU

QnA

